Amendments to the Claims:

This listing of claims will replace all prior versions, and listing of claims in this application:

Listing of Claims:

Claim 1 (Currently Amended) A method comprising:

dispatching an instruction for execution;

speculatively executing said instruction;

determining whether said instruction executed correctly;

routing said instruction to a replay mechanism if said instruction did not execute correctly;

determining whether incorrect execution of said instruction is due to a long latency operation;

routing said instruction for ~~immediate~~ re-execution if said incorrect execution is not due to said long latency operation and advancing said instruction forward for replay into an earlier replay time slot if a slot becomes available;

delaying routing of said instruction for re-execution if said incorrect execution is due to said long latency operation and moving said instruction backwards in time as resource conflicts are detected;

re-executing said instruction if said instruction did not execute correctly; ~~and~~

retiring said instruction if said instruction executed correctly;

routing said instruction to a delay queue to wait a period of time before re-executing said instruction if said incorrect execution is due to said long latency operation;

determining what type of error caused said instruction to execute incorrectly;

predicting what length time period to delay said instruction prior to routing said instruction for re-execution if said incorrect execution is due to said long latency operation;

tracking number of times said instruction is executed and re-executed and increasing said time period to delay said instruction for re-execution as number of time said instruction has been executed and re-executed increases.

Claims 2-6 (Cancelled)

Claim 7 (Currently Amended) The method of claim ~~6~~ 1 wherein said retiring further comprises applying a result of said instruction to an architectural state if said instruction executed correctly.

Claim 8 (Original) The method of claim 7 further comprising discarding execution result of said instruction if said instruction executed incorrectly.

Claim 9 (Currently Amended) A method comprising:

dispatching an instruction;

speculatively executing said instruction;

checking whether said instruction executing correctly and determining whether a long latency type of error caused said instruction to execute incorrectly if said instruction did not execute correctly;

replaying said instruction if said instruction did not execute correctly, wherein said replaying comprises dynamically determining a time period to delay said instruction prior to re-execution and shifting said instruction forward for earlier replay if a time slot becomes available and shifting said instruction backwards for later replay if a resource conflict is detected;

re-executing said instruction after said time period elapsed if said instruction did not execute correctly; and

retiring said instruction if said instruction executed correctly;

routing said instruction to a delay queue to wait for said time period to elapse prior to re-executing said instruction if said long latency type of error caused said instruction to execute incorrectly;

routing said instruction from said delay queue for re-execution after said time period has elapsed; and

tracking the number of times said instruction is executed and re-executed, wherein said time period to delay said instruction for re-execution is increased as the number of times said instruction has been executed and re-executed increases.

Claims 10-12 (Cancelled)

Claim 13 (Currently Amended) The method of claim ~~12~~ 9 wherein said routing of said instruction from said delay queue comprises rescheduling said instruction for re-execution.

Claim 14 (Currently Amended) The method of claim ~~12~~ 9 wherein said routing of said instruction from said delay queue comprises sending said instruction for re-execution without rescheduling said instruction.

Claim 15 (Cancelled)

Claim 16 (Currently Amended) The method of claim ~~15~~ 9 wherein said retiring further comprises applying a result of said instruction to an architectural state if said instruction executed correctly.

Claim 17 (Currently Amended) A processor comprising:

a scheduler to dispatch instructions;

a multiplexor coupled to said scheduler, said multiplexor to receive said instructions from said scheduler;

an execution unit coupled to said multiplexor, said execution unit to execute said instructions;

a checker coupled to said execution unit, said checker to determine whether each instruction has executed correctly; and

a replay mechanism coupled to said checker, said replay mechanism to receive from said checker each instruction that has not executed correctly, said replay mechanism further comprising logic to determine whether a long latency operation caused an incorrectly executed instruction, said logic also to dynamically determine a time period to delay said incorrectly executed instruction if said long latency operation caused said incorrectly executed instruction and wherein said logic increases said time period to delay said incorrectly executed instruction as number of times increases.

Claim 18 (Original) he processor of claim 17 wherein said replay mechanism further comprises a delay queue to store said incorrectly executed instruction for said time period prior to releasing said incorrectly executed instruction to said execution unit for re-execution.

Claim 19 (Original) The processor of claim 18 wherein said replay mechanism further comprises a counter to count a number of times said incorrectly executed instruction is executed and re-executed.

Claim 20 (Cancelled)

Claim 21 (Currently Amended) The processor of claim ~~20~~ 17 further comprising:

a retirement unit coupled to said checker to receive any instructions that have executed correctly, said retirement unit to retire said instructions that have executed correctly;

a first level internal cache coupled to said execution unit; and

a second level internal cache coupled to said execution unit, wherein access time to said second level internal cache is greater than to said first level cache.

Claim 22 (Original) The processor of claim 21 wherein said processor is coupled to an external main memory and to a disk memory.

Claim 23 (Currently Amended) The processor of claim 22 wherein said incorrectly executed instruction is a memory load operation, said memory load instruction operation to cause a memory fetch, said memory fetch to search through a memory hierarchy for requested data, wherein said memory hierarchy is comprised ~~comprises~~ of said first level cache, said second level cache, said external main memory and said disk memory, and wherein said first level cache has the fastest access time and said disk memory has the longest access time.

Claim 24 (Original) The processor of claim 23 wherein each incorrect execution of said memory load instruction causes said memory fetch to access a slower level of memory, and said logic increases said time delay to approximate an access latency to said slower level of memory.

Claim 25-30 (Cancelled)